011906764 **Image available**
WPI Acc No: 1998-323674/199829
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Unit for performing numerical and logical operations in processors,
multi-computer systems, data flow processors, digital signal processors -
has bus unit enabling data to be accessed from or results to be passed to
bus system with automatic synchronisation of several receivers to which
data are sent bus access is decoupled from data processing
Patent Assignee: PACT INFORMATIONSTECHNOLOGIE GMBH (PACT-N); PACT XPP
TECHNOLOGIES AG (PACT-N); ENTIRE INTEREST (ENTI-N); PACT GMBH (PACT-N)
Inventor: MUNCH R; VORBACH M; MUENCH R
Number of Countries: 081 Number of Patents: 012
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19651075	A1	19980610	DE 1051075	A	19961209	199829 B
WO 9826356	A1	19980618	WO 97DE2949	A	19971209	199830
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			WO 97DE2949	A	19971209	

Priority Applications (No Type Date): DE 1051075 A 19961209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19651075	A1		29	G06F-015/80	
WO 9826356	A1	G		G06F-015/78	

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  LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR
  TT UA UG US UZ VN YU ZW
  Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GH GM GR IE
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                    Div ex patent EP 943129
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EP 943129 B1 G   G06F-015/78 Related to application EP 200228401
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                    Based on patent WO 9826356
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  MC NL PT SE
DE 59710383 G   G06F-015/78 Based on patent EP 943129
                    Based on patent WO 9826356

Abstract (Basic): DE 19651075 A
    The unit has a programmable computer unit (EALU) for basic
  mathematical and logical functions. The functions and interconnections
  are programmed in registers, enabling processing of a number of data
  types without reprogramming. A state machine (SM-UNIT) controls the
  computer unit. Registers partially in the form of shift registers exist
  for each operand and the result. Result register data are fed back to
  an input via a multiplexer.
    A bus unit (BM-UNIT) enables data to be accessed from or results to
  be passed to a bus system with automatic synchronization of several
  receivers to which data are sent. Bus access is decoupled from data
  processing, esp. configuration and reconfiguration do not affect the
  data transmitter or receiver. Bus transfers are automatically
  controlled by a state machine (SYNC-UNIT) using handshake lines. Return
  messages allow the status of processing and reconfiguration to be
  monitored.
    ADVANTAGE - System has cascadable computer arrangement which is
  flexibly configured in terms of interconnections and functions.
    Dwg.2/16
Title Terms: UNIT; PERFORMANCE; NUMERIC; LOGIC; OPERATE; PROCESSOR; MULTI;
  COMPUTER; SYSTEM; DATA; FLOW; PROCESSOR; DIGITAL; SIGNAL; PROCESSOR; BUS;
  UNIT; ENABLE; DATA; ACCESS; RESULT; PASS; BUS; SYSTEM; AUTOMATIC;
  SYNCHRONISATION; RECEIVE; DATA; SEND; BUS; ACCESS; DECOUPLE; DATA;
  PROCESS
Derwent Class: Q22; T01
International Patent Class (Main): G06F-009/30; G06F-015/16; G06F-015/78;
  G06F-015/80; H03K-019/177
International Patent Class (Additional): B62D-025/00; G06F-009/302;
  G06F-009/38; G06F-013/38
File Segment: EPI; EngPI
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